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Our Docket No.: 0325.00487

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant:	David J. Green et al.		
Application No.:	09/916,453	Examiner:	Ehichioya, F.
Filed:	July 27, 2001	Art Group:	2172
For:	TECHNIQUES FOR JEDEC FILE INFORMATION INTEGRITY AND PRESERVATION OF DEVICE PROGRAMMING SPECIFICATIONS		

CERTIFICATE OF MAILING

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By: Mary Donna Berkley
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APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit the following Appeal Brief pursuant to 37 C.F.R. §41.37 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §41.20(b)(2). Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, Appellants' legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending and remain rejected. The Appellants hereby appeal the rejection of claims 1-20.

IV. STATUS OF AMENDMENTS

Appellants are appealing a final Office Action issued by the Examiner on September 13, 2004. On November 15, 2004, Appellants filed a Response After Final requesting reconsideration of the rejections. On December 21, 2004, the Examiner issued an Advisory maintaining the rejections. On January 12, 2005, Appellants filed a Notice of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A first embodiment of the present invention (as represented by claim 1) concerns a method (FIG. 3) of generating a file. The method generally comprises the steps of (A) generating a

programming item, (B) storing the programming item and (C) storing at least one of a plurality of parameters. The programming item (inside field 132 in FIG. 2) may be generated (step 140 in FIG. 3) from a plurality of parameters (116 in FIG. 1) that define a program for a programmable logic device (102 in FIG. 1). Generation of the programming item is described in the specification on page 13, lines 11-15. The programming items may be stored (step 142 in FIG. 3) in a programming field (field 132 in FIG. 2) of the file (114 in FIGS. 1 and 2) suitable for programming the programmable logic device (102 in FIG. 1). The at least one of the parameters may be stored (step 142 in FIG. 3) in a non-programming field (field 130 in FIG. 2) of the file. Storage of the programming items and the at lest one parameter is generally described in the specification on page 13, line 16 through page 14, line 2. Details of the file 114 may be found in the specification on page 6, line 13 through page 9, line 12.

A second embodiment of the present invention (as represented by claim 11) concerns a storage medium (memory 122 in FIG. 1) generally comprising a medium and a computer program (software 122 in FIG. 1) for use in a computer (106) to generate a file (114). The medium may distribute the computer program that is readable and executable by the computer. The computer program generally includes the steps of (A) generating a programming item, (B) storing the programming item and (C) storing at least one of a plurality of parameters. The programming item (inside field 132 in FIG. 2) may be generated (step 140 in FIG. 3) from a plurality of parameters (116 in FIG. 1) that define a program for a programmable logic device (102 in FIG. 1). Generation of the programming item is described in the specification on page 13, lines 11-15. The programming items may be stored (step 142 in FIG. 3) in a programming field (field 132 in FIG. 2) of the file (114 in

FIGS. 1 and 2) suitable for programming the programmable logic device (102 in FIG. 1). The at least one of the parameters may be stored (step 142 in FIG. 3) in a non-programming field (field 130 in FIG. 2) of the file. Storage of the programming items and the at lest one parameter is generally described in the specification on page 13, line 16 through page 14, line 2. Details of the file 114 may be found in the specification on page 6, line 13 through page 9, line 12.

A third embodiment of the present invention (as represented by claim 20) concerns a system (100 in FIG. 1) generally comprising (A) means for generating a programming item, (B) means for storing the programming item and (C) means for storing at least one of a plurality of parameters. The means for generating may generate (step 140 in FIG. 3) the programming item (inside field 132 in FIG. 2) from a plurality of parameters (116 in FIG. 1) that define a program for a programmable logic device (102 in FIG. 1). Generation of the programming item is described in the specification on page 13, lines 11-15. The means for generating generally includes a processor 120 and software 122. The first means for storing may store (step 142 in FIG. 3) the programming item in a programming field (field 132 in FIG. 2) of a file (114 in FIGS. 1 and 2) suitable for programming the programmable logic device (102 in FIGS. 1 and 2). The first means for storing generally includes the processor 120, the software 122 and a medium 108. The second means for storing may store (step 142 in FIG. 3) the at least one of the parameters in a non-programming field (field 130 in FIG. 2) of the file. Storage of the programming items and the at lest one parameter is generally described in the specification on page 13, line 16 through page 14, line 2. Details of the file 114 may be found in the specification on page 6, line 13 through page 9, line 12. The second means for storing generally includes the processor 120, the software 122 and the medium 108.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The first issue is whether claim 1 is patentable under the non-statutory double patenting doctrine over co-pending Application No. 09/992,652.

The second issue is whether claims 1, 5, 8-11, 15 and 18-20 are patentable under 35 U.S.C. §103(a) over Schmitz, U.S. Patent No. 5,128,871 in view of Freeman et al., U.S. Patent No. 5,396,505 (hereafter Freeman).

The third issue is whether claims 2-4, 6, 7, 12-14 and 16-17 are patentable under 35 U.S.C. §103(a) over Schmitz and Freeman in view of Schultz et al., U.S. Patent No. 6,255,848 (hereafter Schultz).

VII. ARGUMENTS

A. Non-Statutory Double Patenting

The non-statutory double patenting rejection of claim 1 over claim 1 of co-pending Application No. 09/992,652 appears to be improper. The co-pending application is **not** an issued patent and thus the double patenting **rejection** is inappropriate per MPEP §804.I.A. Furthermore, the Examiner's arguments that a "provisional" double patenting rejection is proper[1] is irrelevant as no **provisional rejection** has been made. Therefore, the non-statutory double patenting rejection of claim 1 should be reversed.

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[1] Advisory Action, December 21, 2004, page 2, "Regarding argument (b-1)" paragraph.

B. 35 U.S.C. § 103

The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness.[2] If the Examiner does not produce a *prima facie* case, the Applicant is under no obligation to submit evidence of non-obviousness.[3] "[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicants."[4] "[T]he factual inquiry whether to combine references must be thorough and searching."[5] "This factual question ... [cannot] be resolved on subjective belief and unknown authority."[6] "It must be based on objective evidence of record."[7] The Examiner must show that (a) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (b) there is a reasonable expectation of success, and (c) the prior art reference (or combination of references) teaches or suggests all of the claim limitations.[8]

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[2] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Rev. 2, May 2004, §2142.

[3] *Id.*

[4] *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316 (Fed. Cir. 2000) (citing *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); *In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)).

[5] *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001).

[6] *In re Lee*, 277 F.3d 1338, 1343-44, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002).

[7] *Id.* at 1343, 61 USPQ2d at 1434.

[8] M.P.E.P. §2142.

The Federal Circuit has held that both the suggestion to modify or combine the references and the reasonable expectation of success must be found in the prior art itself, not merely in Appellant's disclosure.[9] Furthermore, the Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" and must be "clear and particular."[10] Furthermore, the Board has held that the claimed invention is obvious only if either the references expressly or implicitly suggest the claimed invention, or a convincing line of reasoning is presented by the examiner as to why an artisan would have found the claimed invention to be obvious in light of the teachings of the cited references.[11]

1. Rejections over Schmitz and Freeman

a. Claim 1 is fully patentable over Schmitz and Freeman

Claim 1 provides steps for (A) generating a programming item from a plurality of parameters that define a program for a programmable logic device and (B) storing the programming item in a programming field of the file suitable for programming the programmable logic device and (C) storing at least one of the parameters in a non-programming field of the file. Despite the assertion by the Examiner[12] regarding the claimed step (C), column 6, lines 44-67 and column 7 lines 23-32 of Freeman appear to be silent regarding both (i) "parameters" useful for programming a

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[9] See *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991).

[10] *In re Anita Dembiczak* and *Benson Zinbarg*, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999).

[11] See *Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985) (emphasis added by Appellant).

[12] Office Action, September 13, 2004, page 9.

programmable logic device and (ii) storing the parameters in a non-volatile field of a (JEDEC or JEDEC-like) file. The text of Freeman cited by the Examiner reads:

> writing an error checking signal to a unique storage location in a group of NxM storage locations for each one of a set of the MxN possible pairs to said first and second data field values where said group of storage locations is divided into M first data field sets of storage locations, each first data field set including N storage locations with each storage location included in only one first data field set, with each written error checking signal having either a first check value indicating that the possible pair is allowed by the communication protocol or having a second check value indicating that the possible pair is forbidden by the communication protocol;
>
> receiving a given pair of said first and second data fields transmitted on said channel during a particular communication operation;
>
> decoding a received first data field to obtain a first data field value;
>
> utilizing only said first data field value to select a unique one of first data field sets;
>
> ...
>
> a first non-programmable matrix decoder, having row and column inputs for receiving first and second fields respectively and an output for transmitting an unmasked error checking signal selected by said first and second fields received at said inputs, with said error checking signal having either a first check value if the first and second fields are not allowed by the particular hardware configuration and communication protocol or a second check value if the first and second data fields are allowed;

Nowhere in the above text does Freeman appear to discuss storing **a parameter** that defines a program for a programmable logic device **in a non-programming field** of **a file** suitable for programming the programmable logic device. No "parameter" for programming a programmable logic device appears to be mentioned by Freeman. The only "fields" Freeman mentions appear to be part of a communication protocol per column 6, lines 34-36, not part of a file suitable for programming a programmable logic device as presently claimed. The only "non-programming" item mentioned by Freeman appears to be a matrix decoder per column 7, line 23, not a field in a file as

presently claimed. Furthermore, no file suitable for programming a programmable logic device appears to be mentioned by Freeman. Therefore, Schmitz and Freeman, alone or in combination, do not teach or suggest steps for (A) generating a programming item from a plurality of parameters that define a program for a programmable logic device, (B) storing the programming item in a programming field of the file suitable for programming the programmable logic device and (C) storing at least one of the parameters in a non-programming field of the file as presently claimed.

The Examiner fails to provide clear and particular evidence for motivation to combine Schmitz and Freeman. The first asserted motivation that an " 'error checking signal' is used to check if configuration or protocol is changed so that the system can facilitate the reprogramming to compress for the change (see Abstract)"[13] appears to have no applicability to Schmitz. The Examiner provides no evidence or convincing line of reasoning why one of ordinary skill in the art of programmable logic devices would be motivated by a communication protocol invention for configuration and/or protocol changes in a communication system. The Examiner appears to be improperly using the claims as a template to select the references. Therefore, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that "the error checking signal is used to check whether the data fields generated during a particular communication are allowed or forbidden by a communication protocol"[14] does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. Therefore, the second

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[13] Office Action, September 13, 2004, page 4.

[14] Office Action, September 13, 2004, page 9.

asserted motivation appears to be merely a conclusory statement. As such, *prima facie* obviousness has not been established for lack of evidence for motivation.

The Examiner fails to establish a reasonable expectation of success per M.P.E.P. § 2142. In particular, the Examiner is silent regarding any expectation of success. As such, *prima facie* obviousness has not been established for lack of evidence for a reasonable expectation of success.

The references appear to be non-analogous art. Schmitz has a primary U.S. classification of 364/490. Freeman has a primary U.S. classification of 371/57.1. However, no evidence is provided that Freeman is either (i) within the Applicants' field of endeavor or (ii) reasonably pertinent to the particular problem with which the Applicants' were concerned (M.P.E.P. §2141.01(a)). Due to a lack of evidence to the contrary, the U.S. Patent and Trademark Office classifications appear to show that the references are non-analogous art and thus the proposed combination is not obvious.

Furthermore, the assertion by the Examiner[15] that both references "are reasonably pertinent to the particular problem with which the applicants' were concerned" appears to be a conclusory statement not supported by any evidence. As such, *prima facie* obviousness has not been established for lack of evidence that the references are analogous art.

In summary, the Examiner fails to establish that Schmitz and Freeman teach or suggest all of the claim limitations. No clear and particular evidence is provided for motivation to combine or modify the references. No evidence of a reasonable expectation of success is shown. Furthermore, the Examiner fails to establish that the references are analogous art. As such, the rejection of the claimed invention should be reversed.

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[15] Office Action, September 13, 2004, page 4.

b. Claim 11 is fully patentable over Schmitz and Freeman

Claim 11 provides a computer program comprising steps for (A) generating a programming item from a plurality of parameters that define a program for a programmable logic device and (B) storing the programming item in a programming field of the file suitable for programming the programmable logic device and (C) storing at least one of the parameters in a non-programming field of the file. Despite the assertion by the Examiner[16] regarding the claimed step (C), column 6, lines 44-67 and column 7 lines 23-32 of Freeman appear to be silent regarding both (i) "parameters" useful for programming a programmable logic device and (ii) storing the parameters in a non-volatile field of a (JEDEC or JEDEC-like) file. The text of Freeman cited by the Examiner reads:

> writing an error checking signal to a unique storage location in a group of NxM storage locations for each one of a set of the MxN possible pairs to said first and second data field values where said group of storage locations is divided into M first data field sets of storage locations, each first data field set including N storage locations with each storage location included in only one first data field set, with each written error checking signal having either a first check value indicating that the possible pair is allowed by the communication protocol or having a second check value indicating that the possible pair is forbidden by the communication protocol;
>
> receiving a given pair of said first and second data fields transmitted on said channel during a particular communication operation;
>
> decoding a received first data field to obtain a first data field value;
>
> utilizing only said first data field value to select a unique one of first data field sets;
>
> ...
>
> a first non-programmable matrix decoder, having row and column inputs for receiving first and second fields respectively and an output for transmitting an unmasked error checking signal selected by said first and second fields received at said inputs, with said error checking signal having either a first check value if the first and second fields are not

[16] Office Action, September 13, 2004, page 9.

allowed by the particular hardware configuration and communication protocol or a second check value if the first and second data fields are allowed;

Nowhere in the above text does Freeman appear to discuss storing **a parameter** that define a program for a programmable logic device **in a non-programming field** of **a file** suitable for programming the programmable logic device. No "parameter" for programming a programmable logic device appears to be mentioned by Freeman. The only "fields" Freeman mentions appear to be part of a communication protocol per column 6, lines 34-36, not part of a file suitable for programming a programmable logic device as presently claimed. The only "non-programming" item mentioned by Freeman appears to be a matrix decoder per column 7, line 23, not a field in a file as presently claimed. Furthermore, no file suitable for programming a programmable logic device appears to be mentioned by Freeman. Therefore, Schmitz and Freeman, alone or in combination, do not teach or suggest steps for (A) generating a programming item from a plurality of parameters that define a program for a programmable logic device, (B) storing the programming item in a programming field of the file suitable for programming the programmable logic device and (C) storing at least one of the parameters in a non-programming field of the file as presently claimed.

Claim 11 further provides a medium distributing computer program. In contrast, the Examiner fails to provide any evidence in Schmitz and Freeman regarding a computer program in a medium as presently claimed. Furthermore, the assertion by the Examiner[17] that claim 11 is rejected for the same reasons as claim 1 fails to address the structure unique to claim 11. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

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[17] Office Action, September 13, 2004, page 11.

The Examiner fails to provide clear and particular evidence for motivation to combine the references. The first asserted motivation that an " 'error checking signal' is used to check if configuration or protocol is changed so that the system can facilitate the reprogramming to compress for the change (see Abstract)"[18] appears to have no applicability to Schmitz. The Examiner provides no evidence or convincing line of reasoning why one of ordinary skill in the art of programmable logic devices would be motivated by a communication protocol invention for configuration and/or protocol changes in a communication system. The Examiner appears to be improperly using the claims as a template to select the references. Therefore, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that "the error checking signal is used to check whether the data fields generated during a particular communication are allowed or forbidden by a communication protocol"[19] does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. Therefore, the second asserted motivation appears to be merely a conclusory statement. As such, *prima facie* obviousness has not been established for lack of evidence for motivation.

The Examiner fails to establish a reasonable expectation of success per M.P.E.P. § 2142. In particular, the Examiner is silent regarding any expectation of success. As such, *prima facie* obviousness has not been established for lack of evidence for a reasonable expectation of success.

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[18] Office Action, September 13, 2004, page 4.

[19] Office Action, September 13, 2004, page 9.

The references appear to be non-analogous art. Schmitz has a primary U.S. classification of 364/490. Freeman has a primary U.S. classification of 371/57.1. However, no evidence is provided that Freeman is either (i) within the Applicants' field of endeavor or (ii) reasonably pertinent to the particular problem with which the Applicants' were concerned (M.P.E.P. §2141.01(a)). Due to a lack of evidence to the contrary, the U.S. Patent and Trademark Office classifications appear to show that the references are non-analogous art and thus the proposed combination is not obvious.

Furthermore, the assertion by the Examiner[20] that both references "are reasonably pertinent to the particular problem with which the applicants' were concerned" appears to be a conclusory statement not supported by any evidence. As such, *prima facie* obviousness has not been established for lack of evidence that the references are analogous art.

In summary, the Examiner fails to establish that Schmitz and Freeman teach or suggest all of the claim limitations. No clear and particular evidence is provided for motivation to combine or modify the references. No evidence of a reasonable expectation of success is shown. Furthermore, the Examiner fails to establish that the references are analogous art. As such, the rejection of the claimed invention should be reversed.

c. Claim 20 is fully patentable over Schmitz and Freeman

Claim 20 provides means for (A) generating a programming item from a plurality of parameters that define a program for a programmable logic device, means for (B) storing the programming item in a programming field of the file suitable for programming the programmable

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[20] Office Action, September 13, 2004, page 4.

logic device and means for (C) storing at least one of the parameters in a non-programming field of the file. Despite the assertion by the Examiner[21] regarding the means for storing the at least one of the parameters, column 6, lines 44-67 and column 7 lines 23-32 of Freeman appear to be silent regarding both (i) "parameters" useful for programming a programmable logic device and (ii) storing the parameters in a non-volatile field of a (JEDEC or JEDEC-like) file. The text of Freeman cited by the Examiner reads:

> writing an error checking signal to a unique storage location in a group of NxM storage locations for each one of a set of the MxN possible pairs to said first and second data field values where said group of storage locations is divided into M first data field sets of storage locations, each first data field set including N storage locations with each storage location included in only one first data field set, with each written error checking signal having either a first check value indicating that the possible pair is allowed by the communication protocol or having a second check value indicating that the possible pair is forbidden by the communication protocol;
>
> receiving a given pair of said first and second data fields transmitted on said channel during a particular communication operation;
>
> decoding a received first data field to obtain a first data field value;
>
> utilizing only said first data field value to select a unique one of first data field sets;
>
> ...
>
> a first non-programmable matrix decoder, having row and column inputs for receiving first and second fields respectively and an output for transmitting an unmasked error checking signal selected by said first and second fields received at said inputs, with said error checking signal having either a first check value if the first and second fields are not allowed by the particular hardware configuration and communication protocol or a second check value if the first and second data fields are allowed;

Nowhere in the above text does Freeman appear to discuss storing **a parameter** that define a program for a programmable logic device **in a non-programming field** of **a file** suitable for

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[21] Office Action, September 13, 2004, page 9.

programming the programmable logic device. No "parameter" for programming a programmable logic device appears to be mentioned by Freeman. The only "fields" Freeman mentions appear to be part of a communication protocol per column 6, lines 34-36, not part of a file suitable for programming a programmable logic device as presently claimed. The only "non-programming" item mentioned by Freeman appears to be a matrix decoder per column 7, line 23, not a field in a file as presently claimed. Furthermore, no file suitable for programming a programmable logic device appears to be mentioned by Freeman. Therefore, Schmitz and Freeman, alone or in combination, do not teach or suggest means for (A) generating a programming item from a plurality of parameters that define a program for a programmable logic device, means for (B) storing the programming item in a programming field of the file suitable for programming the programmable logic device and means for (C) storing at least one of the parameters in a non-programming field of the file as presently claimed.

Claim 20 further provides a structure comprising a means for generating a programming item, a means for storing the programming item and a means for storing at least one of a plurality of parameters. In contrast, each of Schmitz and Freeman appear to be silent regarding a structure comprising a means for generating a programming item, a means for storing the programming item and a means for storing at least one of a plurality of parameters as presently claimed. Furthermore, the assertion by the Examiner[22] that claim 20 is rejected for the same reasons as claim 1 fails to address the structure unique to claim 20. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

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[22] Office Action, September 13, 2004, page 11.

The Examiner fails to provide clear and particular evidence for motivation to combine the references. The first asserted motivation that an " 'error checking signal' is used to check if configuration or protocol is changed so that the system can facilitate the reprogramming to compress for the change (see Abstract)"[23] appears to have no applicability to Schmitz. The Examiner provides no evidence or convincing line of reasoning why one of ordinary skill in the art of programmable logic devices would be motivated by a communication protocol invention for configuration and/or protocol changes in a communication system. The Examiner appears to be improperly using the claims as a template to select the references. Therefore, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that "the error checking signal is used to check whether the data fields generated during a particular communication are allowed or forbidden by a communication protocol"[24] does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. Therefore, the second asserted motivation appears to be merely a conclusory statement. As such, *prima facie* obviousness has not been established for lack of evidence for motivation.

The Examiner fails to establish a reasonable expectation of success per M.P.E.P. § 2142. In particular, the Examiner is silent regarding any expectation of success. As such, *prima facie* obviousness has not been established for lack of evidence for a reasonable expectation of success.

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[23] Office Action, September 13, 2004, page 4.

[24] Office Action, September 13, 2004, page 9.

The references appear to be non-analogous art. Schmitz has a primary U.S. classification of 364/490. Freeman has a primary U.S. classification of 371/57.1. However, no evidence is provided that Freeman is either (i) within the Applicants' field of endeavor or (ii) reasonably pertinent to the particular problem with which the Applicants' were concerned (M.P.E.P. §2141.01(a)). Due to a lack of evidence to the contrary, the U.S. Patent and Trademark Office classifications appear to show that the references are non-analogous art and thus the proposed combination is not obvious.

Furthermore, the assertion by the Examiner[25] that both references "are reasonably pertinent to the particular problem with which the applicants' were concerned" appears to be a conclusory statement not supported by any evidence. As such, *prima facie* obviousness has not been established for lack of evidence that the references are analogous art.

In summary, the Examiner has fails to establish that Schmitz and Freeman teach or suggest all of the claim limitations. No clear and particular evidence of motivation is provided for motivation to combine or modify the references. No evidence of a reasonable expectation of success is shown. Furthermore, the Examiner fails to establish that the references are analogous art. As such, the rejection of the claimed invention should be reversed.

d. Claims 5 and 15 are fully patentable over Schmitz and Freeman

Claim 5 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 5.

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[25] Office Action, September 13, 2004, page 4.

Claim 15 depends from claim 11 and thus contains all of the limitations of claim 11. Consequently, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 15.

Claim 5 further provides steps for (i)(from claim 1) storing at least one of a plurality of parameters that define a program for a programmable logic device in a non-programming field of a file and (ii)(from claim 5) storing an error detection item in a second non-programming field of the file. Claim 15 provides language similar to claim 5. In contrast, the Examiner cites[26] (i) the same text of Freeman as discussing both a first non-programming field and a second non-programming field and (ii) the same "error checking signal" of Freeman as both the claimed at least one parameter and the claimed error checking item. The text of Freeman cited by the Examiner[27] is reproduced above within the arguments for claim 1. As noted in the arguments for claim 1, the cited text of Freeman does not appear to mention (a) a parameter that defines a program for a programmable logic device, (b) a non-programming field in a file or (c) a file suitable for programming the programmable logic device as presently claimed. Furthermore, the cited text of Freeman does not appear to mention (i) a second non-programming field within a file suitable for programming a programmable logic device and (ii) a parameter, other than the error checking signal of Freeman, as presently claimed. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejections of claims 5 and 15 should be reversed.

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[26] Office Action, September 13, 2004, page 9.

[27] Office Action, September 13, 2004, page 9.

e. Claims 8 and 18 are fully patentable over Schmitz and Freeman

Claim 8 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 8.

Claim 18 depends from claim 11 and thus contains all of the limitations of claim 11. Consequently, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 18.

Claim 8 further provides a step of storing an identification item configured to identify a programmable logic device in a second non-programming field of a file. Claim 18 provides language similar to claim 8. Despite the assertion by the Examiner[28], the text in column 2, lines 44-57 of Schmitz appears to be silent regarding storing an identification item in a second non-programmable field. The cited text of Schmitz reads:

> Design input file 20 contains information describing the circuit to be implemented on the programmable logic device. The information in the design input file varies with the design software used, but one skilled in the art know the required information for the design input file. For example, for PALASM 2 software, a first design input file is used for Boolean equation design and another design input file is used for state machine design.
>
> For Boolean equation design, the design input file for the PALASM 2 software contains two segments, a declaration segment and an equations segment. The declaration segment contains design identification, device and pin data, and optionally string substitutions.

Nowhere in the above text does Schmitz appear to discuss a second non-programming field in a file as presently claimed. Furthermore, the Examiner admits, "Schmitz does not explicitly disclose non-

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[28] Office Action, September 13, 2004, page 10.

programming field."[29] Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claims 8 and 18 should be reversed.

f. Claims 9 and 19 are fully patentable over Schmitz and Freeman

Claim 9 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 9.

Claim 19 depends from claim 11 and thus contains all of the limitations of claim 11. Consequently, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 19.

Claim 9 further provides a step of bracketing a non-programming field of a file with a pair of delimiters. Claim 19 provides language similar to claim 9. Despite the assertion by the Examiner[30], FIG. 26 and the text in column 18, lines 26-31 of Schmitz appear to bracket comments in a **programming field** of a JEDEC file, not a **non-programming field** of a file as presently claimed. The cited text in column 30, lines 9-13 of Schmitz appear to discuss brackets in **a product database (PDB) 121** for chip physical resources of the PLD, not **a non-programming field** of a file as presently claimed. Furthermore, the Examiner admits, "Schmitz does not explicitly teach non-

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[29] Office Action, September 13, 2004, page 9, line 6.

[30] Office Action, September 13, 2004, page 10.

programmable field."[31] Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations. As such, the rejection of claims 9 and 19 should be reversed.

g. Claim 10 is fully patentable over Schmitz and Freeman

Claim 10 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 10.

Claim 10 further provides steps for (i)(from claim 1) storing at least one of a plurality of parameters that define a program for a programmable logic device in a non-programming field of a file, (ii)(from claim 10) storing an error detection item in a second non-programmable field of a file and (iii)(from claim 10) storing another parameter in a third non-programming field of the file. In contrast, the Examiner cites[32] (i) column 6, lines 44-57 of Freeman for both the claimed first non-programming field and the claimed second non-programming field and (ii) column 7, lines 23-25 and column 8, lines 22-25 of Freeman for both the claimed first non-programming field and the claimed third non-programming field. The cited text of Freeman in columns 6 and 7 are reproduced above within the arguments for claim 1. However, the cited text in columns 6 and 7 of Freeman fail to mention (a) a parameter, (b) a first non-programming field, (c) a second non-programming field

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[31] Office Action, September 13, 2004, page 9, line 6.

[32] Office Action, September 13, 2004, pages 9 and 10.

and (d) a file suitable for programming a programmable logic device as presently claimed. Furthermore, the cited text in column 8 of Freeman reads:

> second matrix decoder, having row and column inputs for receiving said first-data field and a third data field respectively and an output for transmitting an unmasked error checking signal selected by said first and third fields received at said inputs, with said error checking signal having either said first check value if the first and third fields are not allowed by the particular hardware configuration and communication protocol said second check value if said first and third data fields are allowed.

Nowhere in the cited text does Freeman appear to discuss (a) another parameter of a program for a programmable logic device, (b) a second non-programmable field of a file and (c) a file suitable for programming the programmable logic device as presently claimed. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Claim 10 further provides a step of bracketing a combination of four non-programming fields with a pair of delimiters. Despite the assertion by the Examiner[33], the text in column 3, lines 42-46 of Freeman appears to be silent regarding bracketing non-programming fields of a file. The cited text of Freeman reads:

> If M is an m-bit data field and N is an n-bit data field then the data fields may encode up to 2^m and 2^n values respectively. The symbols M and N in the above equation represent pairings of the values of a particular pair of M and N fields.

Nowhere in the above text does Freeman appear to discuss bracketing non-programming fields. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

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[33] Office Action, September 13, 2004, page 10.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. In particular, the alleged motivation "that the bracketing specifies the required fields for processing"[34] does not appear to be from either reference of knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. Therefore, *prima facie* obviousness has not been established for lack of evidence for motivation.

Furthermore, the Examiner fails to provide any evidence regarding any expectation of for lack of evidence of a reasonable expectation of success. As such, the rejection of claim 10 should be reversed.

2. Rejections over Schmitz, Freeman and Schultz

a. Claims 2 and 12 are fully patentable over Schmitz, Freeman and Schultz

Claim 2 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are incorporated hereunder in support of claim 2.

Claim 12 depends from claim 11 and thus contains all of the limitations of claim 11. Consequently, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 12.

Claim 2 further provides a step of storing a frequency parameter in a non-programming field of a file. Claim 12 provides language similar to claim 2. In contrast, the cited[35] text in column 20,

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[34] Office Action, September 13, 2004, page 11.

[35] Office Action, September 13, 2004, page 12.

lines 36-67 and column 21, lines 1-6 of Schultz, appears to concern writing a configuration clock frequency to **a command register** 420, not **a non-programming field of a file** as presently claimed. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. The first assertion motivation that "[t]he combination of Schultz with Freeman and Schmitz fairly suggest said second storing comprises storing a frequency parameter in said second non-programming field"[36] does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that a "clock frequency determines the order of bit streams, which is very important in the effective operation of the programmable logic device" does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the second asserted motivation appears to be merely a conclusory statement. Therefore, *prima facie* obviousness has not been established for lack of evidence for motivation. As such, the rejection of claims 2 and 12 should be reversed.

b. Claims 3 and 13 are fully patentable over Schmitz, Freeman and Schultz

Claim 3 depends from claim 1 and thus contains all of the limitations of claim 1. Consequently, the arguments presented above in support of the patentability of claim 1 are

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[36] Office Action, September 13, 2004, page 5, second to last line through page 6.

incorporated hereunder in support of claim 3.

Claim 13 depends from claim 11 and thus contains all of the limitations of claim 11. Consequently, the arguments presented above in support of the patentability of claim 11 are incorporated hereunder in support of claim 13.

Claim 3 further provides steps for (i)(from claim 1) storing at least one of a plurality of parameters that define a program for a programmable logic device in a non-programming field of a file and (ii)(from claim 3) storing a second of the parameters in a second non-programming field of the file. Claim 13 provides language similar to claim 3. The Examiner cites[37] column 7, lines 23-32 of Freeman as teaching both claimed parameters and both claimed non-programming fields. The cited text of Freeman is reproduces above within the arguments for claim 1. However, the cited text of Freeman appears to be silent regarding (a) a first parameter and (b) two non-programming fields as presently claimed. Furthermore, no clear evidence is provided by the Examiner that the above cited text of Freeman teaches two parameters as presently claimed. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. The first assertion motivation that "[t]he combination of Schultz with Freeman and Schmitz fairly suggest said second storing comprises storing a frequency parameter in said second non-programming field"[38] does not appear to be from either reference or knowledge

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[37] Office Action, September 13, 2004, page 12.

[38] Office Action, September 13, 2004, page 5, second to last line through page 6.

generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that a "clock frequency determines the order of bit streams, which is very important in the effective operation of the programmable logic device" does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the second asserted motivation appears to be merely a conclusory statement. Therefore, *prima facie* obviousness has not been established for lack of evidence for motivation. As such, the rejection of claims 3 and 13 should be reversed.

c. Claims 4 and 14 are fully patentable over Schmitz, Freeman and Schultz

Claim 4 depends from claim 3 and thus contains all of the limitations of claim 3. Consequently, the arguments presented above in support of the patentability of claim 3 are incorporated hereunder in support of claim 4.

Claim 14 depends from claim 13 and thus contains all of the limitations of claim 13. Consequently, the arguments presented above in support of the patentability of claim 13 are incorporated hereunder in support of claim 14.

Claim 4 further provides a frequency parameter stored in a second non-programming field of a file suitable for programming a programmable logic device. Claim 14 provides language similar to claim 4. Despite the assertion by the Examiner[39], the text in column 21, lines 2-6 of Schultz appears to be silent regarding a non-programmable field. The cited text of Schultz reads:

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[39] Office Action, September 13, 2004, page 12.

> For example, because the configuration clock frequency is stored by configuration options register 430 and initiated by a command executed in command register 420, the order of these steps in bit stream 900 is determined by configuration circuit 122.

Nowhere in the above text does Schultz appear to discuss non-programming fields of a file suitable for programming a programmable logic device. Therefore, *prima facie* obviousness has not been established for lack of evidence that the references teach all of the claim limitations.

Furthermore, the Examiner fails to provide clear and particular evidence of motivation to combine the references. The first assertion motivation that "[t]he combination of Schultz with Freeman and Schmitz fairly suggest said second storing comprises storing a frequency parameter in said second non-programming field"[40] does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that a "clock frequency determines the order of bit streams, which is very important in the effective operation of the programmable logic device" does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the second asserted motivation appears to be merely a conclusory statement. Therefore, *prima facie* obviousness has not been established for lack of evidence for motivation. As such, the rejection of claims 4 and 14 should be reversed.

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[40] Office Action, September 13, 2004, page 5, second to last line through page 6.

d. Claims 6, 7, 16 and 17 are fully patentable over Schmitz, Freeman and Schultz

Claims 6 and 7 depend from claim 5 and thus contains all of the limitations of claim 5. Consequently, the arguments presented above in support of the patentability of claim 5 are incorporated hereunder in support of claims 6 and 7.

Claims 16 and 17 depend from claim 15 and thus contains all of the limitations of claim 15. Consequently, the arguments presented above in support of the patentability of claim 15 are incorporated hereunder in support of claims 16 and 17.

The Examiner fails to provide clear and particular evidence of motivation to combine the references. The first assertion motivation that "[t]he combination of Schultz with Freeman and Schmitz fairly suggest said second storing comprises storing a frequency parameter in said second non-programming field"[41] does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the first asserted motivation appears to be merely a conclusory statement.

Furthermore, the second asserted motivation that a "clock frequency determines the order of bit streams, which is very important in the effective operation of the programmable logic device" does not appear to be from either reference or knowledge generally available to one of ordinary skill in the art as required by M.P.E.P. §2142. As such, the second asserted motivation appears to be merely a conclusory statement. Therefore, *prima facie* obviousness has not been established for lack of evidence for motivation. As such, the rejection of claims 6, 7, 16 and 17 should be reversed.

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[41] Office Action, September 13, 2004, page 5, second to last line through page 6.

C. CONCLUSION

None of the cited references appear to teach or suggest a step for storing at least one of a plurality of parameters in a non-programming field of the file as presently claimed. Furthermore, *prima facie* obviousness has not been established for lack of clear and particular evidence for motivation to combine or modify the references. Furthermore, Schmitz and Freeman appear to be non-analogous art. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are not rendered obvious by the cited reference. However, should the Board find the arguments herein in support of independent claims 1, 11, and/or 20 unpersuasive, the Board is respectfully requested to carefully consider the arguments set forth above in support of each of the independently patentable groups.

Respectfully submitted,

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VIII. CLAIM APPENDIX

1. A method of generating a file, the method comprising the steps of:

(A) generating a programming item from a plurality of parameters that define a program for a programmable logic device;

(B) storing said programming item in a programming field of said file suitable for programming said programmable logic device; and

(C) storing at least one of said parameters in a non-programming field of said file.

2. The method according to claim 1, wherein step (C) comprises storing a frequency parameter in said non-programming field.

3. The method according to claim 1, further comprising the step of second storing one of said parameters in a second non-programming field of said file.

4. The method according to claim 3, wherein said second storing comprises storing a frequency parameter in said second non-programming field.

5. The method according to claim 1, further comprising the steps of:

generating an error detection item; and

storing said error detection item in a second non-programming field of said file.

6. The method according to claim 5, wherein said error detection item is a cyclic redundancy check checksum.

7. The method according to claim 6, wherein said cyclic redundancy check checksum is configured to detect a bit swap within said file.

8. The method according to claim 1, further comprising the step of storing an identification item configured to identify said programmable logic device in a second non-programming field of said file.

9. The method according to claim 1, further comprising the step of bracketing said non-programming field with a pair of delimiters.

10. The method according to claim 1, further comprising the steps of:

generating an error detection item;

storing said error detection item is a second non-programming field of said file;

storing another of said parameters in a third non-programming field of said file;

storing an identification item in a fourth non-programming field of said file; and

bracketing a combination of said non-programming field, said second non-programming field, said third non-programming field, and said fourth non-programming field with a pair of delimiters.

11. A storage medium comprising a medium and a computer program for use in a computer to generate a file, the medium distributing the computer program that is readable and executable by the computer, the computer program including the steps of:

(A) generating a programming item from a plurality of parameters that define a program for a programmable logic device;

(B) storing said programming item in a programming field of said file suitable for programming said programmable logic device; and

(C) storing at least one of said parameters in a non-programming field of said file.

12. The storage medium according to claim 11, wherein step (C) comprises storing a frequency parameter in said non-programming field.

13. The storage medium according to claim 11, wherein said computer program further comprises the step of second storing one of said parameters in a second non-programming field of said file.

14. The storage medium according to claim 13, wherein said second storing comprises storing a frequency parameter in said second non-programming field.

15. The storage medium according to claim 11, wherein said computer program further comprises the steps of:

generating an error detection item; and

storing said error detection item in a second non-programming field of said file.

16. The storage medium according to claim 15, wherein said error detection item is a cyclic redundancy check checksum.

17. The storage medium according to claim 16, wherein said cyclic redundancy check checksum is configured to detect a bit swap within said file.

18. The storage medium according to claim 11, wherein said computer program further comprises the step of storing an identification item configured to identify said programmable logic device in a second non-programming field of said file.

19. The storage medium according to claim 11, wherein said computer program further comprises the step of bracketing said non-programming field with a pair of delimiters.

20. A system comprising:

means for generating a programming item from a plurality of parameters that define a program for a programmable logic device;

means for storing said programming item in a programming field of a file suitable for programming said programmable logic device; and

means for storing at least one of said parameters in a non-programming field of said file.